

SN5474, SN54LS74A, SN54S74 SN7474, SN74LS74A, SN74S74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 - DECEMBER 1983 - REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C.

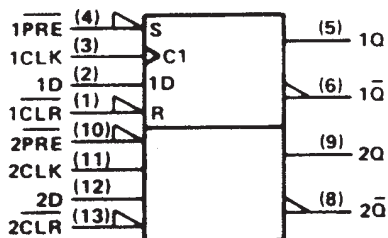
The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [†]	H [†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	\bar{Q}_0

† The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

logic symbol[‡]

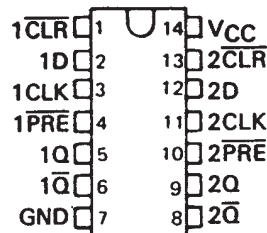


[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

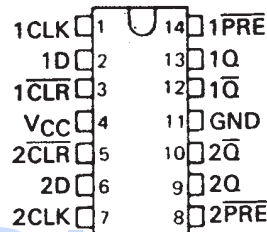
Pin numbers shown are for D, J, N, and W packages.

SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE

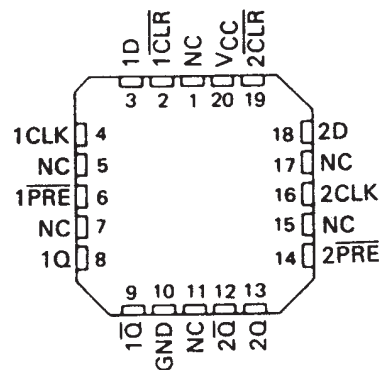
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)

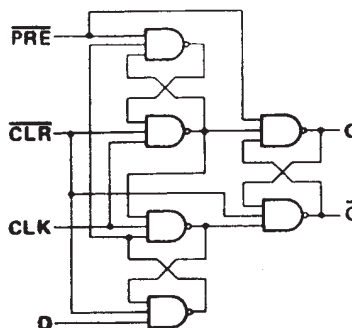


SN54LS74A, SN54S74 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

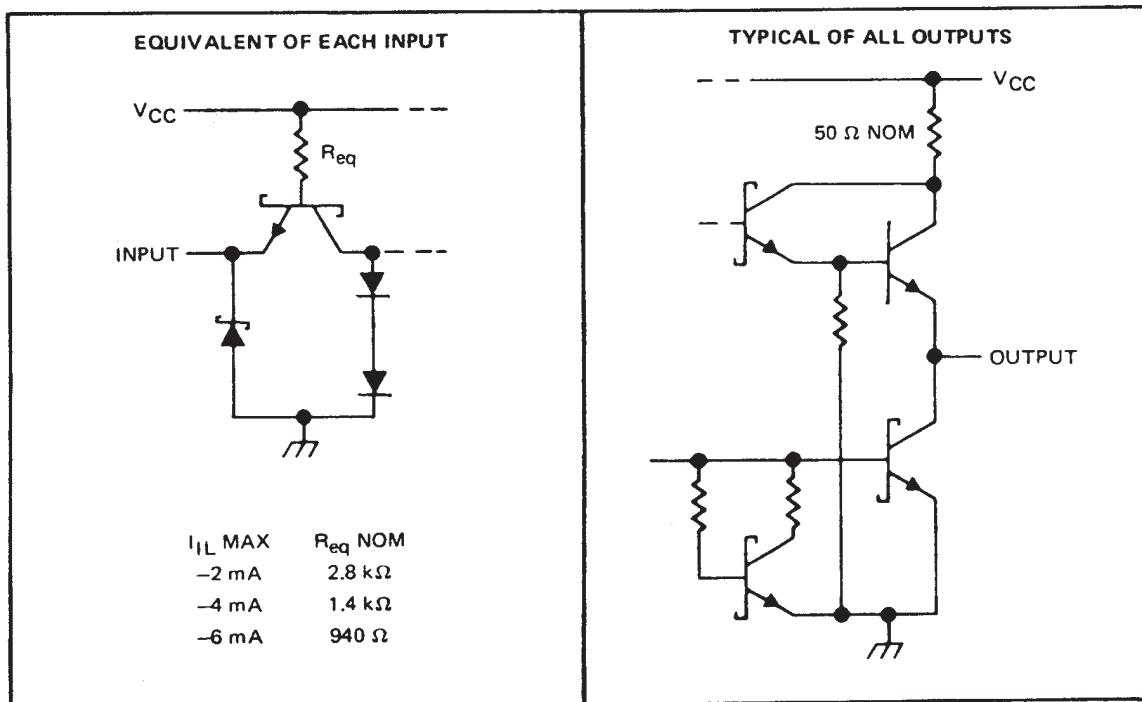
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schematics of inputs and outputs

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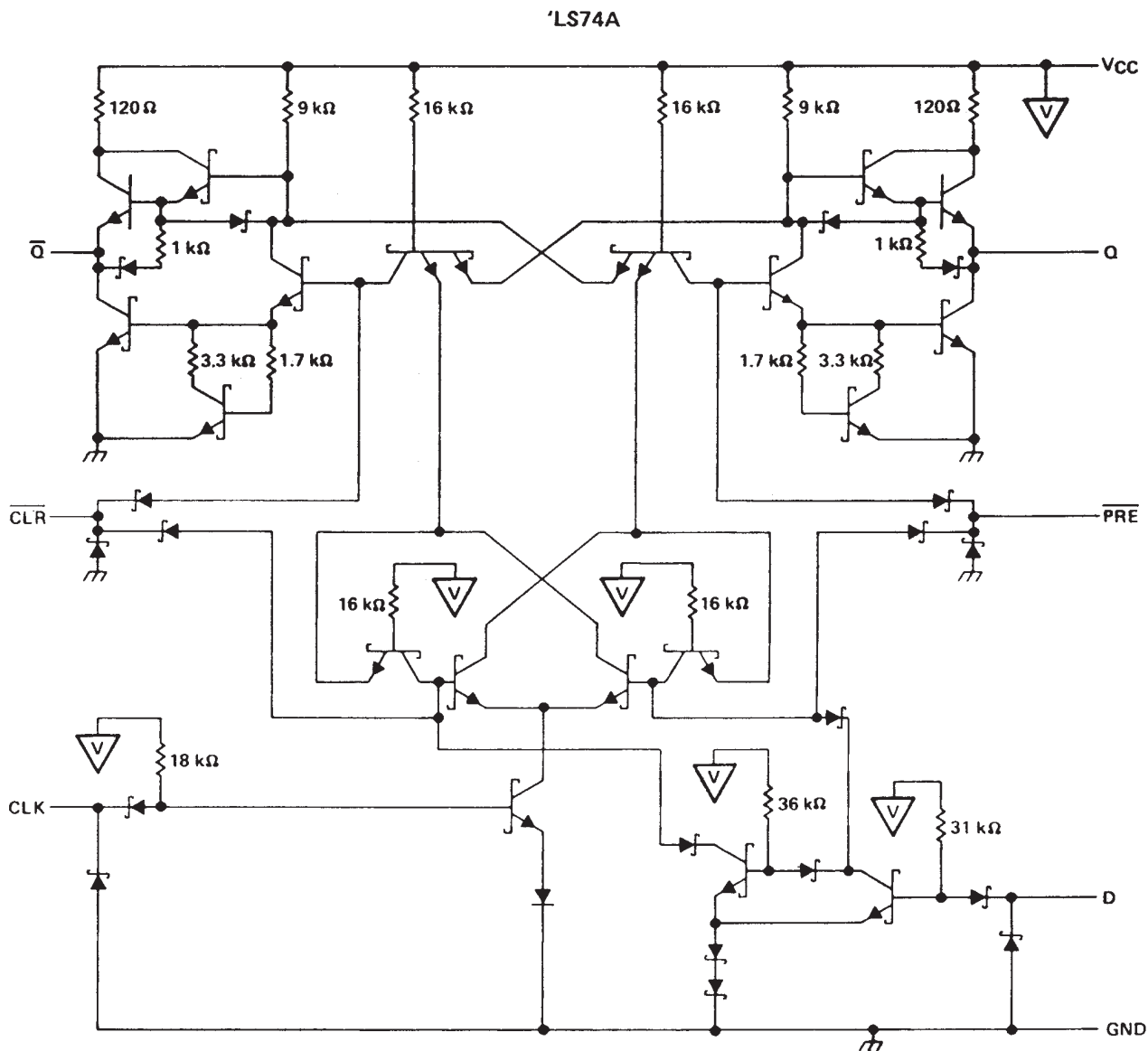
'S74



DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

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schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: '74, 'S74	5.5 V
'LS74A	7 V
Operating free-air temperature range: SN54'	-55 °C to 125 °C
SN74'	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

SN5474, SN54LS74A, SN54S74
SN7474, SN74LS74A, SN74S74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

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recommended operating conditions

		SN5474			SN7474			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			16			16	mA
t _w	Pulse duration	CLK high		30	30		ns	
		CLK low		37	37			
		PRE or CLR low		30	30			
t _{su}	Input setup time before CLK †	20			20			ns
t _h	Input hold time-data after CLK †	5			5			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN5474		SN7474		UNIT		
				MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IK}		V _{CC} = MIN,	I _I = -12 mA			-1.5		-1.5	V	
V _{OH}		V _{CC} = MIN,	V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.4 mA	2.4	3.4		2.4	3.4	V	
V _{OL}		V _{CC} = MIN,	V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2 0.4		0.2	0.4	V	
I _I		V _{CC} = MAX,	V _I = 5.5 V			1		1	mA	
I _{IH}	D	V _{CC} = MAX,	V _I = 2.4 V			40		40	μA	
	CLR					120		120		
	All Other					80		80		
I _{IL}	D	V _{CC} = MAX,	V _I = 0.4 V			-1.6		-1.6	mA	
	PRE‡					-1.6		-1.6		
	CLR‡					-3.2		-3.2		
	CLK					-3.2		-3.2		
I _{OS} †		V _{CC} = MAX		-20		-57		-18	-57	mA
I _{CC} #		V _{CC} = MAX,	See Note 2		8.5	15		8.5	15	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Clear is tested with preset high and preset is tested with clear high.

†Not more than one output should be shown at a time.

#Average per flip-flop.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
f _{max}					15	25		MHz	
t _{PLH}	PRE or CLR	Q or Q̄	R _L = 400 Ω,	C _L = 15 pF			25	ns	
t _{PHL}							40	ns	
t _{PLH}	CLK	Q or Q̄					14	25	ns
t _{PHL}							20	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

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recommended operating conditions

		SN54LS74A			SN74LS74A			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
V _{IH}	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage			0.7			0.8	V	
I _{OH}	High-level output current			-0.4			-0.4	mA	
I _{OL}	Low-level output current			4			8	mA	
f _{clock}	Clock frequency	0		25	0		25	MHz	
t _w	Pulse duration	CLK high		25	25			ns	
		PRE or CLR low		25	25				
t _{su}	Setup time-before CLK ↑	High-level data		20	20			ns	
		Low-level data		20	20				
t _h	Hold time-data after CLK ↑	5		5				ns	
T _A	Operating free-air temperature	-55		125		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS74A			SN74LS74A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA	-1.5			-1.5			V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA					0.35	0.5	
I _I	D or CLK	0.1			0.1			mA
	CLR or PRE	0.2			0.2			
I _{IH}	D or CLK	20			20			μA
	CLR or PRE	40			40			
I _{IL}	D or CLK	-0.4			-0.4			mA
	CLR or PRE	-0.8			-0.8			
I _{OS} §	V _{CC} = MAX, See Note 4	-20		-100	-20		-100	mA
I _{CC} (Total)	V _{CC} = MAX, See Note 2	4		8	4		8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
f _{max}			R _L = 2 kΩ,	C _L = 15 pF	25	33		MHz	
t _{PLH}	CLR, PRE or CLK	Q or Q̄					13	25	ns
t _{PHL}							25	40	ns

Note 3: Load circuits and voltage waveforms are shown in Section 1.

SN5474, SN54LS74A, SN54S74
 SN7474, SN74LS74A, SN74S74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

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recommended operating conditions

		SN54S74			SN74S74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	6.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.8			0.8			V
I _{OH}	High-level output current	-1			-1			mA
I _{OL}	Low-level output current	20			20			mA
t _w	Pulse duration	CLK high		6	6		ns	
		CLK low		7.3	7.3			
		CLR or PRE low		7	7			
t _{su}	Setup time, before CLK ↑	High-level data		3	3		ns	
		Low-level data		3	3			
t _h	Input hold time - data after CLK ↑	2			2			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S74			SN74S74			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA,	-1.2			-1.2			V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA	0.5			0.5			V
I _I		V _{CC} = MAX, V _I = 5.5 V	1			1			mA
I _{IH}	D	V _{CC} = MAX, V _I = 2.7 V	50			50			μA
	CLR		150			150			
	PRE or CLK		100			100			
I _{IL}	D	V _{CC} = MAX, V _I = 0.5 V	-2			-2			mA
	CLR†		-6			-6			
	PRE†		-4			-4			
	CLK		-4			-4			
I _{OS} ‡		V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CC} #		V _{CC} = MAX, See Note 2	15	25		15	25		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

¶Clear is tested with preset high and preset is tested with clear high.

#Average per flip-flop.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			R _L = 280 Ω, C _L = 15 pF	75	110		MHz
t _{PLH}	PRE or CLR	Q or Q̄			4	6	ns
t _{PHL}	PRE or CLR (CLK high)				9	13.5	ns
	PRE or CLR (CLK low)				5	8	
t _{PLH}	CLK	Q or Q̄			6	9	ns
t _{PHL}					6	9	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
JM38510/00205BCA	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
JM38510/00205BDA	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
JM38510/00205BDA	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
JM38510/07101BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/07101BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/07101BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/07101BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30102B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30102B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30102BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30102BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30102BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30102BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30102SCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30102SCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30102SDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30102SDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SN5474J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN5474J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN54LS74AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN54LS74AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN54S74J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN54S74J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN7474DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN7474DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN7474N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7474N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7474N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7474N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS74AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
SN74LS74ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS74AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS74AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS74AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS74AN3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS74AN3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS74ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS74ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS74ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS74ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S74N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S74N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74S74N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74S74NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S74NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S74NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S74NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ5474J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ5474J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ5474W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
SNJ5474W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
SNJ54LS74AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS74AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS74AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS74AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS74AW	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS74AW	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S74FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S74FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S74J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S74J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S74W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S74W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

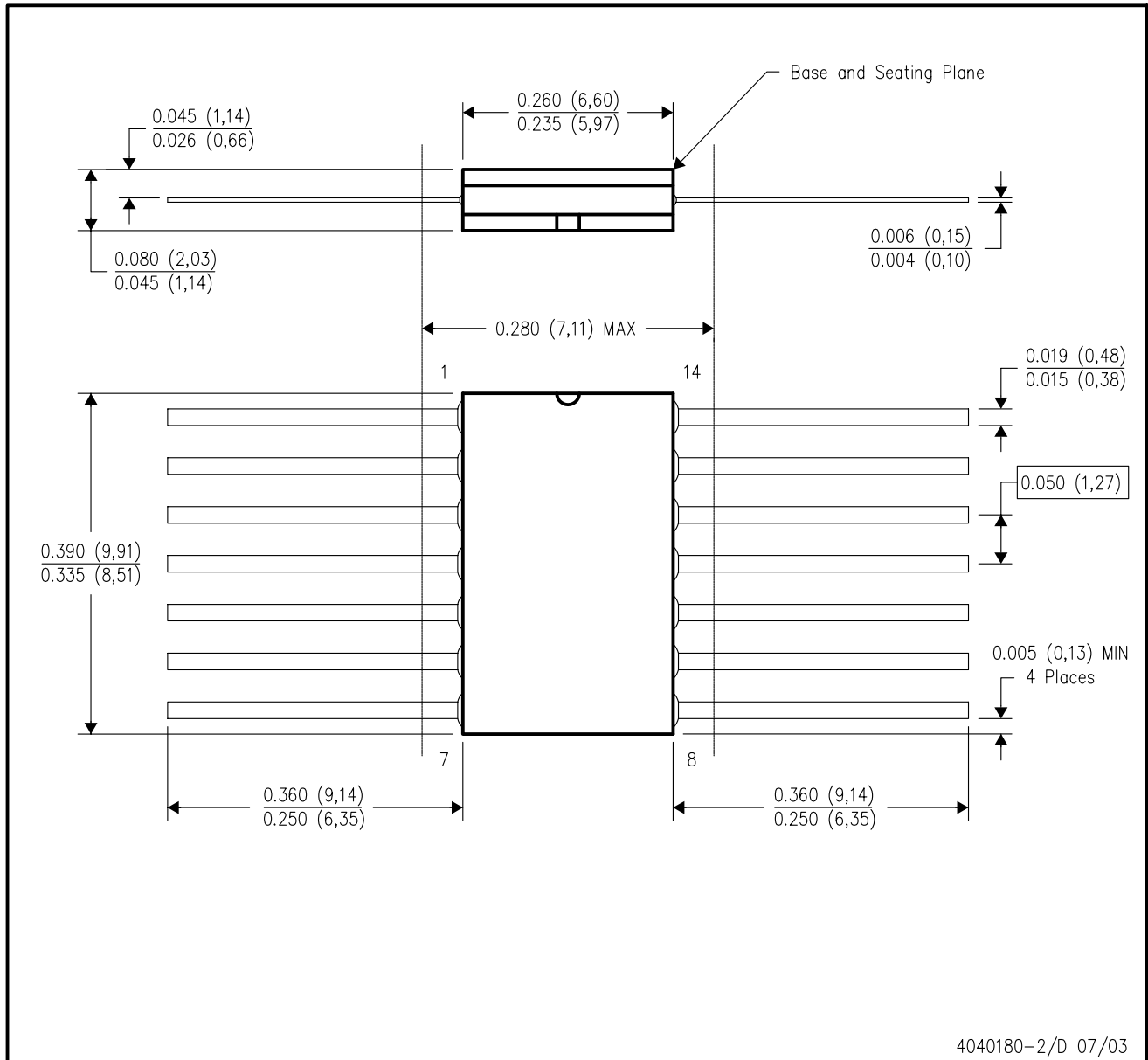


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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View ROHS Compliant Devices

clear gif

SN74LS74A, Status: ACTIVE

View RoHS Compliant Devices

Dual D-type pos.-edge-triggered flip-flops with preset and clear

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<input type="checkbox"/> Features	<input type="checkbox"/> Samples	<input type="checkbox"/> Technical Documents
<input type="checkbox"/> Quality & Pb-Free Data	<input type="checkbox"/> Pricing/Packaging	<input type="checkbox"/> Applications Notes
<input type="checkbox"/> Related Products	<input type="checkbox"/> Inventory	<input type="checkbox"/> Simulation Models
<input type="checkbox"/> Tools & Software	<input type="checkbox"/> Symbols/Footprints	<input type="checkbox"/> Reference Designs

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Refine Your Selection

- Logic: D-Type Flip-Flop

Support

- KnowledgeBase
- Contact Technical Support
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomenclature

Datasheet

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Download Datasheet

Dual D-Type Positive-Edge -Triggered Flip-Flops With Preset And Clear (sn74ls74a.pdf, 699 KB)
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	SN54LS74A	SN74LS74A
Voltage Nodes(V)	5	5
Vcc range(V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive(mA)		-0.4/8
Output	3S	3S
No. of Bits	2	2
Static Current		8
th(ns)		5
tpd max(ns)		40
tsu(ns)		20
	Samples	Samples
	Inventory	Inventory

Product Information

Features Save this to your personal library

Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
Dependable Texas Instruments Quality and Reliability

Description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price (\$US) QTY	Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74LS74AD	ACTIVE	0 to 70	0.29 1KU	SOIC (D) 14	View	50	<input type="checkbox"/>	Purchase Samples
SN74LS74ADBR	ACTIVE	0 to 70	0.29 1KU	SSOP (DB) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LS74ADBRE4	ACTIVE	0 to 70	0.29 1KU	SSOP (DB) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LS74ADE4	ACTIVE	0 to 70	0.29 1KU	SOIC (D) 14	View	50	<input type="checkbox"/>	Purchase Samples
SN74LS74ADR	ACTIVE	0 to 70	0.29 1KU	SOIC (D) 14	View	2500	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LS74ADRE4	ACTIVE	0 to 70	0.29 1KU	SOIC (D) 14	View	2500	<input type="checkbox"/>	Purchase Samples
SN74LS74AJ	OBSOLETE	0 to 70		CDIP (J) 14			<input type="checkbox"/>	Not Available
SN74LS74AN	ACTIVE	0 to 70	0.29 1KU	PDIP (N) 14	View	25	<input type="checkbox"/>	Purchase Samples
SN74LS74AN3	OBSOLETE	0 to 70		PDIP (N) 14	View		<input type="checkbox"/>	Not Available
SN74LS74ANE4	ACTIVE	0 to 70	0.29 1KU	PDIP (N) 14	View	25	<input type="checkbox"/>	Request Free Samples
SN74LS74ANSR	ACTIVE	0 to 70	0.29 1KU	SO (NS) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LS74ANSRG4	ACTIVE	0 to 70	0.29 1KU	SO (NS) 14	View	2000	<input type="checkbox"/>	Purchase Samples

Inventory

		TI Inventory Status			Reported Distributor Inventory			
SN74LS74AD		As of 9:04 AM GMT, 25 Nov 2005			As of 9:04 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
	0*	>10k 27 Feb	14 Weeks	Americas	Avnet	>1k	<input type="text"/>	
					Newark InOne	>1k	<input type="text"/>	
				Europe	Abacus Polar	550	<input type="text"/>	
					Arrow Southern Europe	228	<input type="text"/>	
					EBV Elektronik	550	<input type="text"/>	
SN74LS74ADBR		As of 9:04 AM GMT, 25 Nov 2005			As of 9:04 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
	0*	>10k 9 Feb	11 Weeks	Americas	Avnet	>1k	<input type="text"/>	
SN74LS74ADBRE4		As of 9:04 AM GMT, 25 Nov 2005			As of 9:04 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
	0*	>10k 9 Feb	11 Weeks	None Reported View Distributors				
SN74LS74ADE4		As of 9:04 AM GMT, 25 Nov 2005			As of 9:04 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
	0*	>10k 27 Feb	14 Weeks	None Reported View Distributors				
SN74LS74ADR		As of 9:04 AM GMT, 25 Nov 2005			As of 9:04 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
	0*	>10k 27 Feb	14 Weeks	Americas	DigiKey	>1k	<input type="text"/>	
				Europe	Arrow Southern Europe	>1k	<input type="text"/>	

View all Distributors

Choose a Region



SN74LS74ADRE4	As of 9:04 AM GMT, 25 Nov 2005			As of 9:04 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 27 Feb	14 Weeks	None Reported View Distributors			
SN74LS74AN	As of 9:04 AM GMT, 25 Nov 2005			As of 9:04 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	9750*	>10k 5 Jan	4 Weeks	Americas	Avnet	>1k	<input type="text"/>
					DigiKey	>1k	<input type="text"/>
					Newark InOne	>1k	<input type="text"/>
				Europe	Abacus Polar	>1k	<input type="text"/>
					Arrow Northern Europe	>1k	<input type="text"/>
					Arrow Southern Europe	322	<input type="text"/>
					Avnet- SILICA	>1k	<input type="text"/>
					EBV Elektronik	>1k	<input type="text"/>
					Spoerle	>1k	<input type="text"/>
SN74LS74ANE4	As of 9:04 AM GMT, 25 Nov 2005			As of 9:04 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	9750*	>10k 5 Jan	4 Weeks	None Reported View Distributors			
SN74LS74ANSR	As of 9:04 AM GMT, 25 Nov 2005			As of 9:04 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	585 17 Mar	14 Weeks	None Reported View Distributors			
SN74LS74ANSRG4	As of 9:04 AM GMT, 25 Nov 2005			As of 9:04 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		14 Weeks	None Reported View Distributors			

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Quality & Lead (Pb)-Free Data						
<input type="checkbox"/>	Product Content				MTBF/FIT Rate	
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details	
SN74LS74AD <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LS74ADBR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LS74ADBRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LS74ADE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LS74ADR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LS74ADRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LS74AN <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View	
SN74LS74ANE4 <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View	
SN74LS74ANSR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LS74ANSRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our [Product Information Centers](#) regarding the availability of this information.

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Application Notes

Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB)

08 Jul 2004 [Abstract](#)

Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB)

24 May 2004 [Abstract](#)

Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB)

28 May 2003 [Abstract](#)

TI IBIS File Creation, Validation, and Distribution Processes (szza034.htm, 9 KB)

29 Aug 2002 [Abstract](#)

Designing With Logic (Rev. C) (sdya009c.htm, 9 KB)

01 Jun 1997 [Abstract](#)

Designing with the SN54/74LS123 (Rev. A) (sdla006a.htm, 9 KB)

01 Mar 1997 [Abstract](#)

Live Insertion (sdya012.htm, 9 KB)

01 Oct 1996 [Abstract](#)

Input and Output Characteristics of Digital Integrated Circuits (sdya010.htm, 9 KB)

01 Oct 1996 [Abstract](#)

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User Guides

LOGIC Pocket Data Book (scyd013.pdf, 4835 KB)

05 Dec 2002 [Download](#)

More Literature

Logic Selection Guide 2005 (Rev. X) (sdyu001x.pdf, 6909 KB)

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Military Semiconductors Selection Guide 2004-2005 (Rev. D) (sgyc003d.pdf, 964 KB)

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Logic Cross-Reference (Rev. A) (scyb017a.pdf, 2938 KB)

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