## high efficiency red IPD2545A green IPD2547A yellow IPD2548A

### 0.252" 4-Character $5 \times 7$ Dot Matrix X-Y Stackable Industrial Alphanumeric Programmable Display ${ }^{\text {™ }}$ with Built-in CMOS Control Functions



- Four 0.252" Dot Matrix Characters in Hermetic Package
- Built-in Memory, Decoders, Multiplexer and Drivers
- Viewing Angle, $X$ axis $\pm 40^{\circ}, Y$ axis $\pm 75^{\circ}$
- 128 Character ASCII Format (Upper and Lower Case Characters)
- Rugged Ceramic Package, Hermetic Sealed Flat Glass Window
- Wide Temperature Operating Range for Industrial Use, $-55^{\circ} \mathrm{C}$ to $+100^{\circ} \mathrm{C}$
- 8-bit Bidirectional Data BUS
- READ/WRITE Capability
- Built-in Character Generator ROM
- TTL Compatible
- Easily Cascaded for Multidisplay Operation
- Less CPU Time Required
- Software Controlled Features:
- Programmable Highlight Attribute (Blinking, Non-Blinking)
- Asynchronous Memory Clear Function
- Lamp Test
- Display Blank Function
- Single or Multiple Character Blinking Function
- Three Programmable Brightness Levels



## DESCRIPTION

The IPD2545A (high efficiency red), IPD2547A (green), and IPD2548A (yellow) are four digit, High Reliability/Industrial, dot matrix, Programmable Displays that are aimed at satisfying the most demanding industrial display requirements.
They are designed for use in harsh environments. The devices are constructed in a hermetic package using four 0.25 -inch high $5 \times 7$ dot matrix displays.
The devices incorporate the latest in CMOS technology which is the heart of the device intelligence. The CMOS controller chip is controlled by a user supplied eight bit data word on the bidirectional BUS. The ASCII data and attribute data are word driven. This approach allows the IPD254XA to interface using the same techniques as a microprocessor peripheral.
Applications include: control panels, night viewing applications (red light), cockpit monitors, night vision goggle viewable displays (green), portable and vehicle technology as well as industrial controllers.

## Maximum Ratings

DC Supply Voltage -0.5 to +6.0 Vdc Input Voltage Relative to Ground (all inputs) -0.5 to $V_{C C}+0.5 \mathrm{Vdc}$
Operating Temperature
$\qquad$ .$-55^{\circ} \mathrm{C}$ to $100^{\circ} \mathrm{C}$
Storage Temperature $\qquad$ $-65^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$
Thermal Resistance ( $\theta_{\mathrm{JC}}$ ). $30^{\circ} \mathrm{C} / \mathrm{N}$

## Important:

Refer to Appnote 18, "Using and Handling Intelligent Displays". Since this is a CMOS device, normal precautions should be taken to avoid static damage.

Figure 1. Top View


## Pin Assignments

| 1 | $\overline{\text { RD }}$ | Read | 11 | $\overline{\text { WR }}$ | Write |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 2 | CLK I/O | Clock I/O | 12 | D7 | Data MSB |
| 3 | $\overline{\text { CLKSEL }}$ | Clock Select | 13 | D6 | Data |
| 4 | $\overline{\text { RST }}$ | Reset | 14 | D5 | Data |
| 5 | CE1 | Chip Enable | 15 | D4 | Data |
| 6 | $\overline{\text { CE0 }}$ | Chip Enable | 16 | D3 | Data |
| 7 | A2 | Address MSB | 17 | D2 | Data |
| 8 | A1 | Address | 18 | D1 | Data |
| 9 | A0 | Address LSB | 19 | D0 | Data LSB |
| 10 | GND | - | 20 | $V_{C C}$ | - |

Figure 2. Timing Characteristics—Data "Write" Cycle


Figure 3. Timing Characteristics-Data "Read" Cycle


Notes:

1. All input voltages are $V_{\mathrm{IL}}=0.8 \mathrm{~V}, V_{\mathrm{IH}}=2.0 \mathrm{~V}$.
2. These waveforms are not edge triggered.

## DC Characteristics

| Parameter | $-55^{\circ} \mathrm{C}$ |  |  | $+25^{\circ} \mathrm{C}$ |  |  | $+100^{\circ} \mathrm{C}$ |  |  | Units | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. |  |  |
| $I_{\text {CC }}$ Blank | - | 4.0 | 10 | - | 2.0 | 5.0 | - | 1.0 | 2.5 | mA | $\begin{aligned} & V_{\mathrm{CC}}=5.0 \mathrm{~V} \\ & \left(\mathrm{~A}_{2}=1\right. \\ & \text { all other inputs low) } \end{aligned}$ |
| $I_{\text {CC }}$ | - | 220 | 250 | - | 160 | 190 | - | 125 | 160 | mA | $V_{C C}=5.0 \mathrm{~V}, 20$ dots/digit, (100\% brightness) |
| $I_{\text {IL }}$ (all inputs) | - | 70 | 120 | - | 60 | 100 | - | 50 | 80 | $\mu \mathrm{A}$ | $V_{\mathrm{CC}}=5.0 \mathrm{~V}, V_{\mathrm{IH}}=0.8 \mathrm{~V}$ |
| $V_{\mathrm{IH}}$ (all inputs) | 2.0 | - | - | 2.0 | - | - | 2.0 | - | - | V | $V_{\text {CC }}=5.0 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |
| $V_{\text {IL }}$ (all inputs) | - | - | 0.8 | - | - | 0.8 | - | - | 0.8 | V | $V_{\text {CC }}=5.0 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |

[^0]IPD2545A/7A/8A

## Optical Characteristics

## High Efficiency Red IPD2545A

| Description | Symbol | Min. | Typ.(4) | Units | Test Condition |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Peak Luminous Intensity per LED ${ }^{(1,3)}$ <br> (Character Average) | IVave | 75 | 150 | $\mu \mathrm{~cd}$ | $V_{\mathrm{CC}}=5.0 \mathrm{~V}$, \# sign "ON" on all digits at <br> full brightness, $T_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |
| Peak Wavelength | $\lambda_{\text {peak }}$ | - | 635 | nm | - |
| Dominant Wavelength (2) | $\lambda_{\text {dom }}$ | - | 626 | nm | - |

## High Efficiency Green IPD2547A

| Description | Symbol | Min. | Typ. ${ }^{(4)}$ | Units | Test Condition |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Peak Luminous Intensity per LED <br> (1,3) <br> (Character Average) | $\mathrm{I}_{\text {Vave }}$ | 75 | 150 | $\mu \mathrm{~cd}$ | $V_{\mathrm{CC}}=5.0 \mathrm{~V}$, \# sign "ON" on all digits at <br> full brightness, $T_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |
| Peak Wavelength | $\lambda_{\text {peak }}$ | - | 568 | nm | - |
| Dominant Wavelength (2) | $\lambda_{\text {dom }}$ | - | 574 | nm | - |

Yellow IPD2548A

| Description | Symbol | Min. | Typ.(4) | Units | Test Condition |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Peak Luminous Intensity per LED <br> (1,3) <br> (Character Average) | $\mathrm{I}_{\text {Vave }}$ | 75 | 150 | $\mu \mathrm{~cd}$ | $V_{\mathrm{CC}}=5.0 \mathrm{~V}$, \# sign "ON" on all digits at <br> full brightness, $T_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |
| Peak Wavelength | $\lambda_{\text {peak }}$ | - | 585 | nm | - |
| Dominant Wavelength (2) | $\lambda_{\text {dom }}$ | - | 590 | nm | - |

Notes:

1) The displays are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
${ }^{2)}$ Dominant wavelength $\lambda_{\text {dom }}$ is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2) The luminous stearance of the LED may be calculated using the following relationships.
$\mathrm{L}_{\mathrm{V}}\left(\mathrm{cd} / \mathrm{m}^{2}\right)=\mathrm{I}_{V}\left(\right.$ Candela) $/ \mathrm{A}(\text { Meter })^{2}$
$\mathrm{L}_{\mathrm{V}}($ Footlamberts $)=\pi \mathrm{I}_{\mathrm{V}}\left(\right.$ Candela) $/ \mathrm{A}(\text { Foot })^{2}$
$A=8.4 \times 10^{-7} \mathrm{ft}^{2}, 7.8 \times 10^{-8} \mathrm{~m}^{2}$
3) All typical values specified at $V_{\mathrm{CC}}=5.0 \mathrm{~V}$ and $T_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise noted.

## Pin Definitions

| Pin | Function | Definition |
| :--- | :--- | :--- |
| 1 | $\overline{\text { RD }}$ | Active low, will enable a processor to read <br> all registers. |
| 2 | CLK I/O | If CLK SEL (pin 3) is low, then expect an <br> external clock source into this pin. If CLK <br> SEL is high, then this pin will be the master <br> or source for all other devices which have <br> CLK SEL low. |
| 3 | $\overline{\mathrm{CLKSEL}}$ | CLocK SELect determines the action of pin <br> 2, CLK I/O. See section on Cascading for an <br> example. |
| 4 | $\overline{\text { RST }}$ | Reset. The Reset pulse should be less than <br> 1 ms. Reset is used only to synchronize <br> blinking and will not clear the display. |
| 5 | CE1 | Chip enable (active high). <br> 6 <br> $\overline{\mathrm{CEO}}$ |
| 7 | A2 | Chip enable (active low). |
| 8 | A1 | Address input (MSB). |

Pin Definitions (continued)

| Pin | Function | Definition |
| :--- | :--- | :--- |
| 9 | A0 | Address input (LSB). |
| 10 | GND | Ground. |
| 11 | $\overline{\text { WR }}$ | Write. Active low. If the device is selected, <br> a low on the write input loads the data into <br> memory. |
| 12 | D7 | Data Bus bit 7 (MSB). |
| 13 | D6 | Data Bus bit 6. |
| 14 | D5 | Data Bus bit 5. |
| 15 | D4 | Data Bus bit 4. |
| 16 | D3 | Data Bus bit 3. |
| 17 | D2 | Data Bus bit 2. |
| 18 | D1 | Data Bus bit 1. |
| 19 | D0 | Data Bus bit 0 (LSB). |
| 20 | $V_{C C}$ | Positive power pin. |

Switching Specifications ( $V_{\mathrm{CC}}=4.5 \mathrm{~V}$ )

| Write Cycle Timing |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter | Description | Specification Minimum |  |  |  |
|  |  | $-55{ }^{\circ} \mathrm{C}$ | $+25^{\circ} \mathrm{C}$ | $+100^{\circ} \mathrm{C}$ | Units |
| $T_{\text {CLR }}{ }^{(1)}$ | Clear RAM | 1.0 | 1.0 | 1.0 | $\mu \mathrm{s}$ |
| $T_{\text {CLRD }}{ }^{(1)}$ | Clear RAM Disable | 1.0 | 1.0 | 1.0 | $\mu \mathrm{s}$ |
| $T_{\text {AS }}$ | Address Setup | 10 | 10 | 10 | ns |
| $T_{\text {CES }}$ | Chip Enable Setup | 0 | 0 | 0 | ns |
| $T_{\mathrm{RS}}$ | Read Enable Setup | 10 | 10 | 10 | ns |
| $T_{\mathrm{DS}}$ | Data Setup | 20 | 30 | 50 | ns |
| $T_{\mathrm{W}}$ | Write Pulse | 60 | 70 | 90 | ns |
| $T_{\text {AH }}$ | Address Hold | 20 | 30 | 40 | ns |
| $T_{\text {DH }}$ | Data Hold | 20 | 30 | 40 | ns |
| $T_{\text {CEH }}$ | Chip Enable Hold | 0 | 0 | 0 | ns |
| $T_{\mathrm{RH}}$ | Read Enable Hold | 20 | 30 | 40 | ns |
| $T_{\text {ACC }}$ | Total Access Time = Setup Time + Write Time + Hold Time | 90 | 110 | 140 | ns |

Switching specifications ( $V_{\mathrm{CC}}=4.5 \mathrm{~V}$ )
Read Cycle Timing

| Parameter | Description | Specification Minimum |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | -55 ${ }^{\circ} \mathrm{C}$ | $+25^{\circ} \mathrm{C}$ | $+100^{\circ} \mathrm{C}$ | Units |
| $T_{\text {AS }}$ | Address Setup | 0 | 0 | 0 | ns |
| $T_{\text {CES }}$ | Chip Enable | 0 | 0 | 0 | ns |
| $T_{\text {WS }}$ | Write Enable Setup | 20 | 30 | 40 | ns |
| $T_{\text {DD }}$ | Data Delay Time | 100 | 150 | 175 | ns |
| $T_{\mathrm{R}}$ | Read Pulse | 150 | 175 | 200 | ns |
| $T_{\text {AH }}$ | Address Hold | 0 | 0 | 0 | ns |
| $T_{\text {DH }}$ | Data Hold | 0 | 0 | 0 | ns |
| $T_{\text {TRI }}$ | Time to Tristate (Max. time) | 30 | 40 | 50 | ns |
| $T_{\text {CEH }}$ | Chip Enable Hold | 0 | 0 | 0 | ns |
| $T_{\text {WH }}$ | Write Enable Hold | 30 | 40 | 50 | ns |
| $T_{\text {RACC }}$ | Total Access Time = Setup Time + Read Time + Time to Tristate | 200 | 245 | 290 | ns |
| $T_{\text {WAIT }}{ }^{(1)}$ | Wait Time between Reads | 0 | 0 | 0 | ns |

## Notes:

${ }^{1)}$ Wait $1.0 \mu \mathrm{~s}$ between any Reads or Writes after writing a Control Word with a Clear (D7=1). Wait $1.0 \mu \mathrm{~s}$ between any Reads or Writes after Clearing a Control Word with a Clear (D7=0). All other Reads and Writes can be back to back.
2) All input voltages are ( $V_{\mathrm{IL}}=0.8 \mathrm{~V}, V_{\mathrm{IH}}=2.0 \mathrm{~V}$ )
3) Data out voltages are measured with 100 pF on the data bus and the ability to source $=-40 \mu \mathrm{~A}$ and sink $=1.6 \mathrm{~mA}$ The rise and fall times are $60 \mathrm{~ns} . V_{\mathrm{OL}}=0.4 \mathrm{~V}, V_{\mathrm{OH}}=2.4 \mathrm{~V}$.

Figure 4. Block Diagram


## Functional Description

The block diagram (Figure 4) includes 5 major blocks and internal registers (indicated by dotted lines).
Display Memory consists of a $5 \times 8$ bit RAM block. Each of the four 8-bit words holds the 7-bits of ASCII data (bits D0-D6) and an attribute select bit (Bit D7). The fifth 8-bit memory word is used as a control word register. A detailed description of the control register and its functions can be found under the heading Control Word. Each 8-bit word is addressable and can be read from or written to.

## Mode Selection

| $\overline{\mathbf{C E O}}$ | $\mathbf{C E 1}$ | $\overline{\mathbf{R D}}$ | $\overline{\mathbf{W R}}$ | Operation |
| :--- | :--- | :--- | :--- | :--- |
| 0 | 1 | 0 | 0 | None |
| 1 | $X$ | $X$ | $X$ | None |
| $X$ | 0 | $X$ | $X$ | None |
| $X$ | $X$ | 1 | 1 | None |

$0=$ Low logic level, $1=$ High logic level, $X=$ Don't care

The Control Logic dictates all of the features of the display device and is discussed in the Control Word section of this data sheet.

The Character Generator converts the 7-bit ASCII data into the proper dot pattern for the 128 characters shown in the character set chart.
The Clock Source can originate either from the internal oscillator clock or from an external source-usually from the output of another IPD2545/7/8A in a multiple module display.
The Display Multiplexer controls all display output to the digit drivers so no additional logic is required for a display system.
The Column Drivers are connected directly to the display.
The Display has four digits. Each of the four digits is comprised of 35 LEDs in a $5 \times 7$ dot array which makes up the alphanumeric characters.
The intensity of the display can be varied by the Control Word in steps of $0 \%$ (Blank), $25 \%, 50 \%$, and full brightness.
The Reset pin when activated clears the internal counter. A reset is usually done after power up and is of very short duration-nanoseconds or microseconds. If the reset pin is held low for a longer time (milliseconds) some or all LEDs in the bottom row may light up.
The appearance of lit LEDs during a "reset" is not an indication of a malfunctioning part. It is advisable to keep the reset pulse as short as possible to avoid displaying a row of lit LEDs.

## Microprocessor Interface

The interface to the microprocessor is through the address lines. (A0-A2), the data bus (D0-D7), two chip select lines (CE0, CE1), and read ( $\overline{\mathrm{RD}}$ ) and write ( $\overline{\mathrm{WR})}$ lines.
The $\overline{\mathrm{CEO}}$ should be held low when executing a read, or write operation. CE1 must be held high.
The read and write lines are both active low. During a valid read the data lines (D0-D7) become outputs. A valid write will enable the data lines as inputs.

## Input Buffering

If a cable length of 6 inches or more is used, all inputs to the display should be buffered with a tri-state non-inverting buffer mounted as close to the display as conveniently possible. Recommended buffers are: 74LS245 for the data lines and 74LS244 for the control lines.

## Data Input Commands

| $\overline{\text { CEO }}$ | CE1 | $\overline{\mathbf{R D}}$ | $\overline{\text { WR }}$ | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | No Change |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | Read Digit 0 Data to Bus |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | (\$) Written to Digit 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | (W) Written to Digit 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | (f) Written to Digit 2 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | (3) Written to Digit 3 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | X | X | X | X | X | X | X | Char. Written to Digit 0 and Cursor Enabled |

## Programming the IPD2545/7/8A

There are five registers within the IPD2545/7/8A display. Four of these registers are used to hold the ASCII/attribute code of the four display characters. The fifth register is the Control Word, which is used to blink, blank, clear, or dim the entire display, or to change the presentation (attributes) of individual characters.

## Addressing

The addresses within the display device are shown below. Digit 0 is the rightmost digit of the display, while Digit 3 is on the left. Although there is only one Control Word, it is duplicated at the four address locations 0-3. Data can be read from any of these locations. When one of these locations is written to, all of them will change together.

| Address |  |  | Contents |
| :--- | :--- | :--- | :--- |
| A2 | A1 | A0 |  |
| 0 | X | X | Control Word |
| 1 | 0 | 0 | Digit 0 (rightmost) |
| 1 | 0 | 1 | Digit 1 |
| 1 | 1 | 0 | Digit 2 |
| 1 | 1 | 1 | Digit 3 (leftmost) |

Bit D7 of any of the display digit locations is used to allow an attribute to be assigned to that digit. The attributes are discussed in the next section. If Bit D7 is set to a one, that character will be displayed using the attribute. If bit D7 is cleared, the character will display normally.

## Control Word

When address bit A2 is taken low, the Control Word is accessed. The same Control Word appears in all four of the lower address spaces of the display. Through the Control Word, the display can be cleared, the lamps can be tested, display brightness can be selected, and attributes can be set for any characters which have been loaded with their most significant bit (D7) set high.
Brightness (D0, D1): The state of the lower two bits of the Control Word are used to set the brightness of the entire display, from 0\% to $100 \%$. The table below shows the correspondence of these bits to the brightness.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | $X$ | $X$ | $X$ | $X$ | 0 | 0 | Blank |
| 0 | 0 | $X$ | $X$ | $X$ | $X$ | 0 | 1 | $25 \%$ brightness |
| 0 | 0 | $X$ | $X$ | $X$ | $X$ | 1 | 0 | $50 \%$ brightness |
| 0 | 0 | $X$ | $X$ | $X$ | $X$ | 1 | 1 | Full brightness |

X=don't care
Attributes (D2-D4): Bits D2, D3, and D4 control the visual attributes (i.e., blinking, alternate) of those display digits which have been written with bit D7 set high. In order to use any of the four attributes, the Cursor Enable bit (D4 in the Control Word) must be set. When the Cursor Enable bit is set, and bit D7 in a character location is set, the character will take on one of the following display attributes.

Figure 5. Control Word Format


| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 0 | X | X | B | B | Disable highlight <br> attribute |
| 0 | 0 | 0 | 1 | 0 | 0 | B | B | Display cursor* <br> instead of <br> character |
| 0 | 0 | 0 | 1 | 0 | 1 | B | B | Blink single <br> character |
| 0 | 0 | 0 | 1 | 1 | 0 | B | B | Display blinking <br> cursor* instead <br> of character |
| 0 | 0 | 0 | 1 | 1 | 1 | B | B | Alternate charac- <br> ter with cursor* |

*"Cursor" = all dots in a single character space lit to half brightness X=don't care
$B=$ depends on the selected brightness
Attributes are non-destructive. If a character with bit D7 set is replaced by a cursor (Control Word bit D4 is set, and D3=D2=0) the character will remain in memory and can be revealed again by clearing D4 in the Control Word.
Blink (D5): The entire display can be caused to blink at a rate of approximately 2.0 Hz by setting bit D5 in the Control Word. This blinking is independent of the state of D7 in all character locations.
To synchronize the blink rate in a bank of these devices, it is necessary to tie all devices' clocks and resets together as described in a later section of this data sheet.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 1 | $X$ | $X$ | $X$ | $B$ | $B$ | Blinking display |

Lamp Test (D6): When the Lamp Test bit is set, all dots in the entire display are lit at half brightness. When this bit is cleared, the display returns to the characters that were showing before the lamp test.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 1 | 0 | 0 | $X$ | $X$ | $X$ | $X$ | Lamp test |

Clear Data (D7): When D7 (D7=1) is set in the Control Word, all display memory bits are reset to zero. A second Control Word must be written into the chip with D7 (D7=0) reset to set up attributes and brightness levels.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 1 | 0 | $X$ | $X$ | $X$ | $X$ | $X$ | $X$ | Clear |

## Cascading

Cascading the display (Figure 6) is a simple operation. The requirements for cascading are: 1) decoding the correct address to determine the chip select for each additional device, 2) assuring that all devices are reset simultaneously, and 3) selecting one display as the clock source and setting all others to accept clock input (the reason for cascading the clock is to synchronize the flashing of multiple displays). One display as a source is capable of driving six other displays. If more displays are required, a buffer will be necessary. The source display must have pin 3 tied high to output clock signals. All other displays must have pin 3 tied low.

## Voltage Transients

It has become common practice to provide $0.01 \mu \mathrm{~F}$ bypass capacitors liberally in digital systems. Like other CMOS circuitry, the Intelligent Display controller chip has very low power consumption and the usual $0.01 \mu \mathrm{~F}$ would be adequate were it not for the LEDs. To prevent power supply transients, capacitors with low inductance and high capacitance at high frequencies are required. This suggests a solid tantalum or ceramic disc for high frequency bypass. For larger displays, distribute the bypass capacitors evenly, keeping capacitors as close to the power pins as possible. We recommend a $10 \mu \mathrm{~F}$ and $0.01 \mu \mathrm{~F}$ for every Intelligent Display to decouple the displays themselves, at the display.

Figure 6. Cascading the Display


## How to Load Information into the IPD25545/7/8A

Information loaded into the IPD2545/7/8A can be either ASCII data or Control Word data. The following procedure (see also Typical Loading Sequence) will demonstrate a typical loading sequence and the resulting visual display. The word STOP is used in all of the following examples.

## Set Brightness

Step 1 Set the brightness level of the entire display to your preference (example: 100\%).

## Load Four Characters

Step 2 Load a "S" in the left hand digit.
Step 3 Load a " $T$ " in the next digit.
Step 4 Load an " $O$ " in the next digit.
Step 5 Load a " $P$ " in the right hand digit. If you loaded the information correctly, the IPD2545A now should show the word "STOP."

## Blink a Single Character

Step 6 Into the digit, second from the right, load the hex code "CF," which is the code for an " O " with the D7 bit added as a control bit.

## Note:

The " O " is the only digit which has the control bit (D7) added to normal ASCII data.
Step 7 Load enable blinking character into the control word register. The display now should show "STOP" with a flashing " O ".

## Add Another Blinking Character

Step 8 Into the left hand digit, load the hex code "D3" which gives an "S" with the D7 bit added as a control bit. The display should show "STOP" with flashing " O " and a flashing "S."

## Alternate Character/Cursor Enable

Step 9 Load enable alternate character/cursor into the control word register. The display now should show "STOP" with the "O" and the "S" alternating between the letter and cursor (all dots lit).

## Initiate Four Character Blinking

(Regardless of Control Bit setting)
Step 10 Load enable display blinking. The display now should show the entire word "STOP" blinking.

## Electrical and Mechanical Considerations

The CMOS IC of the IPD2545/7/8A are designed to provide resistance to both Electrostatic and Discharge Damage and Latch Up due to voltage or current surges. Several precautions are strongly recommended for the user, to avoid overstressing these built-in safeguards.

## ESD Protection

Users of the IPD2545/7/8A should be careful to handle the devices consistent with standard ESD protection procedures. Operators should wear appropriate wrist, ankle or feet ground straps and avoid clothing that collects static charges. Work surfaces, tools and transport carriers that come into contact with unshielded devices or assemblies also should be appropriately grounded.

## Latch up Protection

Latch up is condition that occurs in CMOS ICs after the input protection diodes have been broken down. These diodes can be reversed through several means.
$V_{\text {IN }}<\mathrm{GND}, V_{\text {IN }}>V_{\mathrm{CC}}+0.5 \mathrm{~V}$, or through excessive currents begin forced on the inputs. When these situations exist, the IC may develop the response of an SCR and begin conducting as much as one amp through the $V_{C C}$ pin. This destructive condition will persist (latched) until device failure or the device is turned off.
The Voltage Transient Suppression Techniques and buffer interfaces for longer cable runs help considerably to prevent latch conditions from occurring. Additionally, the following Power Up and Power Down sequence should be observed.

## Typical Loading Sequence

|  | $\overline{\text { CEO }}$ | CE1 | $\overline{\mathbf{R D}}$ | $\bar{W} \mathbf{R}$ | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Display |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1. | L | H | H | L | L | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |  |
| 2. | L | H | H | L | H | H | H | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | S |
| 3. | L | H | H | L | H | H | L | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | ST |
| 4. | L | H | H | L | H | L | H | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | STO |
| 5. | L | H | H | L | H | L | L | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | STOP |
| 6. | L | H | H | L | H | L | H | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | STOP |
| 7. | L | H | H | L | L | X | X | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | STO*P |
| 8. | L | H | H | L | H | H | H | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | S*TO*P |
| 9. | L | H | H | L | L | X | X | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | StTOtP |
| 10. | L | H | H | L | L | X | X | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | S*T* ${ }^{*}{ }^{*}{ }^{*}$ |

* Blinking character, $\dagger$ Character alternating with cursor (all dots lit)


## Power up Sequence

1. Float all active signals by tri-stating the inputs to the displays.
2. Apply $V_{C C}$ and GND to the display.
3. Apply active signals to the displays by enabling all input signals per applications.

## Power Down Sequence

1. Float all active signals by tri-stating the inputs to the displays.
2. Turn off the power to the display.

Figure 7. Character Set


Notes:

1. High=1 level
2. Low=0 level
3. Upon power up, the device will initialize in a random state
4. A2 must be held high for ASCII data.
5. Bit $D 7=1$ enables attributes for the assigned digit

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