MIL-PRF-38534 AND 38535 CERTIFIED FACILITY

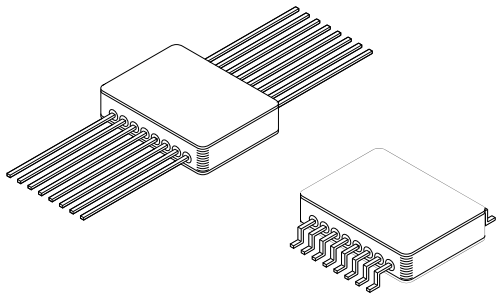
RAD HARD HIGH VOLTAGE SYNCHRONOUS SWITCHING REGULATOR CONTROLLER

5055RH SERIES

M.S.KENNEDY CORP.
4707 Dey Road Liverpool, N.Y. 13088 (315) 701-6751

FEATURES:

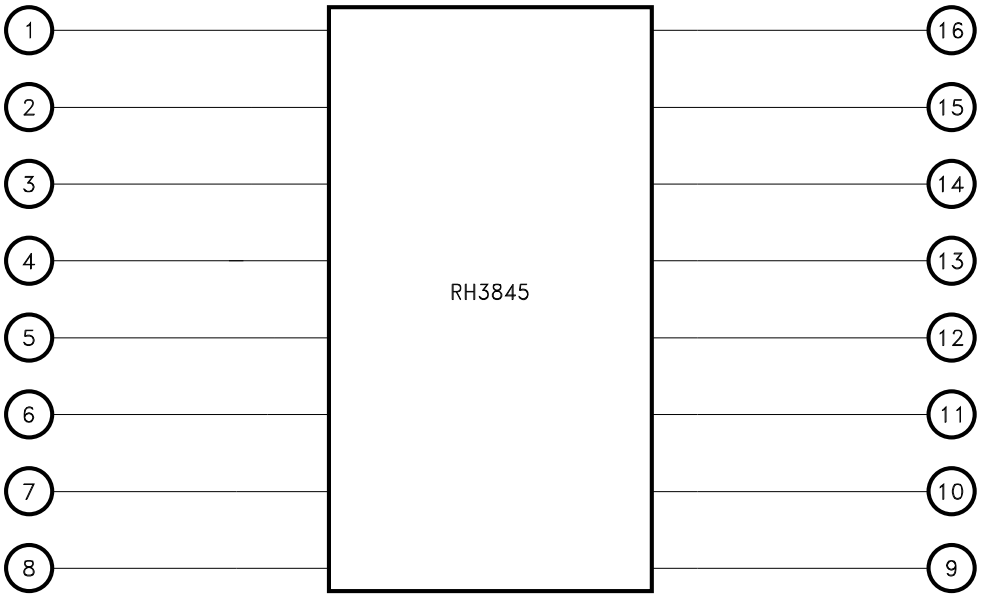
- Manufactured using LINEAR TECHNOLOGY Space Qualified RH3845 Dice
- Radiation Hardened to 300 Krad(Si) (Method 1019.7 Condition A)
- Neutron Tested to 5E11 n/cm² (Method 1017.2)
- High Voltage Operation: Up to 60V Input, and 36V Output
- Programmable Frequency 100-500KHz, or Synchronizable to 600KHz
- 70μA Shutdown Supply Current
- Antislope Compensation – Current Limit Unaffected by Duty Cycle
- Reverse Inductor Current Inhibit – Improves Efficiency with Light Loads
- External Compensation
- Capable of Driving Standard Power MOSFETs
- Equivalent Non Rad Hard Device MSK 5033
- Contact MSK for MIL-PRF-38534 Qualification Status



DESCRIPTION:

The MSK 5055RH is a radiation hardened wide input voltage range step-down synchronous switching regulator controller. The wide input range, programmable output voltage and switching frequency, make these regulators suitable for a wide variety of medium to high power applications. The adjustable operating frequency provides the flexibility to keep the switching noise out of sensitive frequency bands, and when synchronized, can be ganged out of phase with other controllers for reduced noise and component size. The MSK 5055RH is hermetically sealed in a 16 pin flatpack, and is available with straight or gull wing leads.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- POL Applications
- Intermediate Bus Converter
- Satellite System Power Supply
- Step Down Synchronous Regulator
- High Efficiency Subsystem Supply

PIN-OUT INFORMATION

1	VIN	16	BOOST
2	$\overline{\text{SHDN}}$	15	TG
3	CSS	14	SW
4	SGND	13	VCC
5	VFB	12	BG
6	VC	11	PGND
7	SYNC	10	SENSE+
8	FSET	9	SENSE-

CASE = ISOLATED

ABSOLUTE MAXIMUM RATINGS ⑩

V_{IN}	Input Voltage	65V	
V_{BOOST}	BOOST Voltage (BOOST)	80V	
SW	Switch Voltage. ⑨	65V to -2V	
	Differential Boost Voltage (BOOST TO SW)	24V	
VCC	Bias Supply Voltage	24V	
V_{SENSE}	SENSE+ and SENSE- Voltages	40V	
	Differential Sense Voltage	+/-1V	
	SYNC, VC, VFB, CSS and $\overline{SHDN}$	5V	
	$\overline{SHDN}$ Pin Currents	1mA	
T_{LD}	Lead Temperature Range (10 Seconds)	300°C	
T_{ST}	Storage Temperature	-65°C to 150°C	
T_J	Junction Temperature	150°C	
T_C	Operating Case Temperature	-55°C to +125°C	

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions ①⑪		Group A Subgroup	MSK 5055K/H RH Min.	MSK 5055K/H RH Typ.	MSK 5055K/H RH Max.	MSK 5055RH Min.	MSK 5055RH Typ.	MSK 5055RH Max.	Units
VIN Min Start Voltage			1,2,3	-	-	7.5	-	-	7.5	V
VIN UVLO Threshold (Falling)			1,2,3	3.6	3.7	4	3.6	3.7	4	V
		Post 100 Krad(Si)	1	3.55	3.6	4	3.55	3.6	4	V
		Post 300 Krad(Si)	1	3.45	3.5	4	3.45	3.5	4	V
VIN Supply Current②	VCC≥9V		1	-	130	-	-	130	-	uA
VIN Shutdown Current ②	$V_{\overline{SHDN}}$=0V		1,2,3	-	65	-	-	65	-	uA
BOOST Supply Current ② ③			1	-	1.6	-	-	1.6	-	mA
VCC Supply Current			1,2,3	-	4	6	-	4	6	mA
VCC Current Limit			1,2,3	40	150	-	40	150	-	mA
Error Amp Reference Voltage	VC=VFB		1	1.224	1.233	1.238	1.224	1.233	1.238	V
			2,3	1.215	-	1.245	-	-	-	V
		Post 100 Krad(Si)	1	1.200	1.222	1.238	1.200	1.222	1.238	V
		Post 300 Krad(Si)	1	1.173	1.197	1.238	1.173	1.197	1.238	V
VFB Pin Input Current ②	VFB=V_{REF}		1	-	35	-	-	35	-	nA
$\overline{SHDN}$ Enable Threshold (Rising)			1,2,3	1.3	1.37	1.4	1.3	1.37	1.4	V
		Post 300 Krad(Si)	1	1.25	1.3	1.4	1.25	1.3	1.4	V
$\overline{SHDN}$ Threshold Hysteresis②			1	-	125	-	-	125	-	mV
Current Limit Sense Voltage	(V_{SENSE+})-(V_{SENSE-}), VFB=0V		1,2,3	90	109	115	90	109	115	mV
		Post 100 Krad(Si)	1	90	103	115	90	103	115	mV
		Post 300 Krad(Si)	1	84	92	115	84	92	115	mV
Input Current (I_{SENSE+})+(I_{SENSE-}) ②	$V_{SENSE\ (CM)}$=0V		1	-	705	-	-	705	-	uA
Operating Frequency	R_{SET}=49.9KΩ		4,5,6	270	300	330	270	300	330	KHz
		Post 100 Krad(Si)	4	255	295	330	255	295	330	KHz
		Post 300 Krad(Si)	4	250	289	330	250	289	330	KHz
Programmable Frequency Range	F_{SW}≤100kHz at R_{SET}=232KΩ F_{SW}≤500kHz at R_{SET}=22.1KΩ		7,8a,8b	Pass	-	-	Pass	-	-	Pass/Fail
External Sync Frequency Range	100kHz≤F_{SYNC}≤600kHz		7,8a,8b	Pass	-	-	Pass	-	-	Pass/Fail
Sync Voltage Threshold			1,2,3	-	1.4	2	-	1.4	2	V
Soft-Start Capacitor Control Current ②			1	-	11	-	-	11	-	uA
Error Amp Transconductance②			1,2,3	-	400	-	-	400	-	uS
Error Amp DC Voltage Gain ②			1	-	62	-	-	62	-	dB
Error Amp Sink/Source Current ②			1	-	±40	-	-	±40	-	uA
TG, BG Drive On Voltage ② ④	C_{LOAD}=3300pF		1	-	8.5	-	-	8.5	-	V
TG, BG Drive Off Voltage②	C_{LOAD}=3300pF		1	-	0	-	-	0	-	V
TG, BG Drive Rise/Fall Time ②	10% to 90% or 90% to 10% C_{LOAD}=3300pF		4	-	60	-	-	60	-	ns
Minimum TG Off Time			4,5,6	-	290	650	-	290	650	ns
Minimum TG On Time			4,5,6	-	230	400	-	230	400	ns
Gate Drive Nonoverlap Time ②	TG Fall to BG Rise		4	-	245	-	-	245	-	ns
	TG Fall to TG Rise		4	-	125	-	-	125	-	ns
Thermal Resistance②	Junction to Case @ 125°C		-	-	4.8	5.6	-	4.8	5.6	°C/W

NOTES:

① Unless otherwise specified VIN=20V, VCC=BOOST=10V, $\overline{SHDN}$≥2V, R_{SET}=49.9KΩ, SENSE-=SENSE+=10V, SGND=PGND=SW=SYNC=0V.
② Guaranteed by design but not tested. Typical parameters are representative of device performance but are for reference only.
③ Supply current specification does not include switch drive currents. Actual supply currents will be higher.
④ DC measurement of gate drive output "ON" voltage is typically 8.6V. Internal dynamic bootstrap operations yields typical gate "ON" voltages of 9.8V during standard switching operation. Standard operation gate "ON" voltage is not tested but guaranteed by design.
⑤ Industrial grade devices shall be tested to subgroup 1 unless otherwise specified.
⑥ Military grade devices ("H" and "K" suffix) shall be 100% tested to subgroups 1,2,3,4 and 7.
⑦ Subgroup 3,6 and 8 available upon request.
⑧ Subgroup 1,4,7 TC = +25°C
Subgroup 2,5,8a TC = +125°C
Subgroup 3,6,8b TC = -55°C
⑨ The -2V absolute maximum on the SW pin is a transient condition. It is guaranteed by design, but not tested.
⑩ Continuous operation at or above absolute maximum ratings may adversely affect the device performance and/or life cycle.
⑪ Pre and post irradiation limits at 25°C, up to 300 Krad(Si) TID, are identical unless otherwise specified.

APPLICATION NOTES

DEVICE TYPES (-1, -2)

The MSK5055RH can be ordered to operate in one of two different ways at light load. The different modes are internally configured at the factory and are identified by the "dash number."

DASH NUMBER	MODE Internal Connection	Reverse Current Mode
-1	VFB	Disabled (DCM
-2	VCC	Enabled (CCM)

Device type "-1" disables the reverse current capability at light loads. This configuration is more efficient than configuration "-2." It allows the inductor current to go discontinuous and the PWM will skip pulses to maintain regulation at light loads. This configuration will have a minimum load current requirement, typically 1mA.

Device type "-2" allows reverse current in the synchronous switch at light loads. This configuration is less efficient at light loads but operations in continuous conduction mode at light loads.

PIN FUNCTIONS

VIN – The VIN pin is the input supply pin for the device, and should be decoupled to SGND with a low ESR capacitor located close to the pin — (See application circuit for typical values).

VCC – The VCC pin provides access to the internal 8V bias supply for decoupling and optional external sourcing. It is the power supply for most of the internal functions and the MOSFET gate drive. VCC can only source current and may be tied to an external source to improve efficiency and allow for lower voltage operation. If VCC is tied to an external source greater than 6.5V the device will operate with Vin as low as 4V. This configuration reduces power dissipation in the device by bypassing the internal regulator. The VCC pin charges the bootstrapped capacitor through a diode connected to the BOOST pin. In shutdown mode the VCC pin sinks 20μA until the pin voltage is discharged to zero volts. Note: When connecting VCC to an external source. The source must be greater than or equal to VIN +1V.

TG – The TG pin is the gate drive for the forward switch, or top N-Channel MOSFET. Be aware of the high speed and large currents here during circuit layout. Keep traces short and as wide as possible to minimize parasitic impedances.

BG – The BG pin is the gate drive for the synchronous rectifier or bottom N-Channel MOSFET. Be aware of the high speed and large currents here during circuit layout. Keep traces short and as wide as possible to minimize parasitic impedances.

PGND – The PGND pin is the high-current ground reference. Connect it directly to the negative side of the VCC decoupling capacitor. Care should be taken to make sure that these currents are not referenced by the SGND pin to avoid injecting noise into the ground reference.

SGND – the SGND pin should be connected to the negative side of the output capacitor. Use a common ground plane to minimize impedance, but locate the high current fast switching devices together so their returns remain local and do not corrupt the SGND reference.

SW – The SW pin is the switch node for the device. The source of the top MOSFET (forward switch), the drain for the bottom MOSFET (synchronous rectifier), the inductor, and the BOOST capacitor are all connected to this node. Use short wide trace to minimize the impedance of this node.

$\overline{\text{SHDN}}$ – The $\overline{\text{SHDN}}$ pin provides a method to disable the device. Pull this pin below 1.35V (nominal) to disable switching. Pull below one V_{BE} (0.7V nominal) to enter low power shutdown. A resistor divider to VIN can be used to set UVLO using the 1.35V threshold. When not in use, pull the pin up to VIN with a large value resistor. When exceeding the absolute maximum rating of 5V the pin voltage will be clamped at 6V nominal. Limit the current into the pin to less than 1mA to prevent overstress.

BOOST – The BOOST pin provides the supply for the bootstrapped gate drive, and is externally connected to a low ESR ceramic BOOST capacitor. The value of the BOOST capacitor should be at least 50 times greater than the gate capacitance of the top MOSFET. Smaller values may be used, but analysis of the voltage drop is recommended. An external diode connected from VCC to the BOOST pin charges the bootstrap capacitor during the off-time of the main power switch. Locate the VCC and BOOST decoupling capacitors in close proximity to the device.

CSS – The CSS pin is used for soft start. It allows the user to program the rate of change of the output at start-up. The capacitance required for a given output slew rate can be calculated using the following formula:

$$CSS = 11\mu A(T_{SS}/1.231V)$$

The pin should be left open if not in use.

APPLICATION NOTES CONT'D

SENSE$^-$- The SENSE$^-$ pin is the negative input to the current sense amplifier. The sensed inductor current limit is set to 100mV across both SENSE inputs.

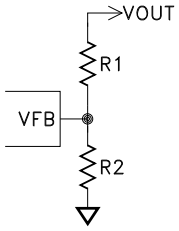
$R_{SENSE} = 70mV/I_{OUT(MAX)}$
Given:
$I_{P-P} < 0.30 \times I_{OUT(MAX)}$

SENSE$^+$ - The SENSE$^+$ pin is the positive input to the current sense amplifier. The sensed inductor current limit is set to 100mV across both SENSE inputs.

$R_{SENSE} = 70mV/I_{OUT(MAX)}$
Given:
$I_{P-P} < 0.30 \times I_{OUT(MAX)}$

VFB – The VFB (Feedback) pin is used to set the output voltage. Use a resistive divider to set the voltage at the VFB pin to 1.231V when the output is at the desired level.

$$V_O = VFB\left[1 + \frac{R1}{R2}\right]$$



VC – The VC pin provides a means to externally compensate the loop response of the controller. VC is the output of the transconductance error amplifier. A capacitor to ground creates a pole in the control loop. A series RC creates a pole zero combination in the control loop. If the VC pin is externally manipulated, use a source impedance of 1KΩ.

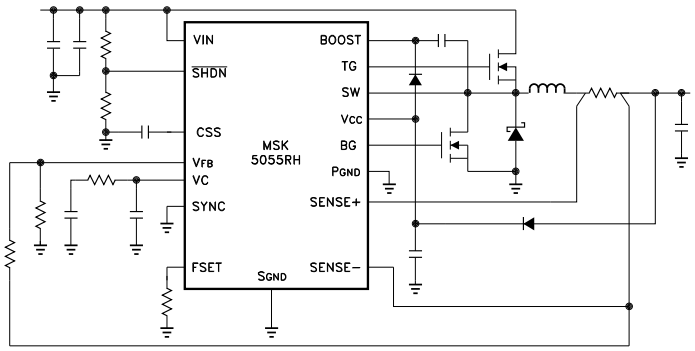
FSET – The FSET pin programs the oscillator frequency via a single resistor to ground. The R_{SET} resistor must be present even when synchronization mode is used—Use the formula or the table below to select the resistance value for a desired frequency.

$$R_{SET}(K\Omega) \approx 8.4 \times 10^4 \times f_{SW(KHZ)}^{(-1.31)}$$

RSET (KΩ)	FSW (KHz)
191	100
118	150
80.6	200
63.4	250
49.9	300
40.2	350
33.2	400
27.4	450
23.2	500

SYNC – The SYNC pin is the input for synchronization of the internal oscillator to an external clock. Program the internal oscillator to be between 10% and 25% below the external clock. The recommended signal is a square wave of at least 2V in amplitude, a pulse width greater than 1μS, and a rise time of less than 500nS. If the SYNC pin is not used in the application, tie it to SGND.

TYPICAL APPLICATION CIRCUIT



SELECTING THE SWITCHING FREQUENCY

The MSK5055RH can be set to operate over a frequency range of 100KHz to 500KHz, and is synchronizeable up to 600KHz. There are several factors to consider when selecting the operating frequency including: efficiency, component size, output ripple, application sensitive frequency bands, and the minimum on time of the controller. The output ripple voltage and efficiency will vary with frequency and input voltage. Higher frequencies increase switching losses, but use smaller inductors and/or bulk capacitors saving board space. Lower frequencies reduce switching losses, but increase ripple current and require larger inductors and/or bulk capacitance to achieve the same output ripple voltage.

SELECTING THE INPUT CAPACITOR

The input capacitance provides a low impedance source to the input of the regulator. A low impedance is necessary for high speed, high efficiency switching and tight regulation. The input bus sources an average DC current while the input capacitance sources the AC component of the input current. Select the input capacitor based on voltage ripple requirements, RMS current rating and bulk capacitance. Assuming the capacitor ESR is lower than the bus impedance at the switching frequency and above, the ESR will dominate the voltage ripple.

$V_{P-P} \cong I_{P-P} \times ESR$
Given: $I_{P-P} = I_{OUT}$

The RMS current capability is related to power dissipation capability of the capacitor. Replace the capacitor with one that has a higher rating, or place more capacitors in parallel if more capability is needed. Sharing of ripple current between capacitors will be approximately equal if all of the capacitors are the same type, and preferably from the same lot. The RMS current seen by the input capacitors can be approximated by the following equation:

$I_{RMS} \cong I_{OUT} \times SQRT\ (3D\text{^}2 - 3D + 1)$
Given: $D \cong V_{OUT}/V_{IN}$

Parallel ceramic capacitors are required to filter the high frequency components of the switching waveform. Locate the bias supply capacitors close to the VIN and SGND pins on the MSK5055RH. Locate the power input capacitors close to the drain of the forward switch (VIN) and the source of the synchronous rectifier (Power Ground). Use short, wide PCB lands to minimize parasitic impedances.

APPLICATION NOTES CONT'D

SELECTING THE OUTPUT CAPACITOR

The output capacitor filters the ripple current from the inductor to an acceptable ripple voltage seen by the load. The primary factor in determining voltage ripple is the ESR of the output capacitor. The voltage ripple can be approximated as follows:

$$V_{P-P} = I_{P-P} \times ESR$$

The capacitive term of the output voltage ripple lags the ESR term by 90° and can be calculated as follows:

$$V_{P-P(CAP)} = I_{P-P} / (8 \times f \times c)$$

Where:
C = output capacitance in Farads

Select a capacitor or combination of capacitors that can tolerate the worst-case ripple current with sufficient de-rating. When using multiple capacitors in parallel to achieve lower ESR or more bulk capacitance, sharing of ripple current between capacitors will be approximately equal if all of the capacitors are the same type, and preferably from the same lot. Low ESR tantalum capacitors are recommended over aluminum electrolytic capacitors. Use ceramic decoupling capacitors to minimize high frequency noise.

COMPENSATING THE LOOP

The feedback loop response can be optimized for the application by adjusting the values of the RC network from the V_C pin to ground. Analysis is recommended to determine the phase margin and gain margin at the specific input voltage and load conditions of the application. Typically, a single RC network from VC to ground works well. An additional ceramic capacitor from VC to ground may be needed to cancel the zero and prevent high frequency ringing or instability.

SELECTING THE INDUCTOR

The important parameters for inductor selection are: its value, volt-second product, saturation and RMS current. To determine the peak current in the inductor add ½ of the p-p ripple current to the desired $I_{OUT(MAX)}$. A typical starting point for peak to peak current ripple is 20% of $I_{OUT(MAX)}$. Use the following equation to determine the RMS current:

$$I_{RMS} = I_{DC} * SQRT (1 + (1/3) * (\Delta I/I_{DC})^2)$$

Given:
I_{DC} = The DC output current
ΔI = ½ of the peak to peak ripple current
The minimum inductance value can be calculated as follows:

$$L_{MIN} > V_{OUT} \times \frac{2DC_{MAX}-1}{DC_{MAX}} \times \frac{R_{SENSE} \times 8.33}{f_{SW}}$$

Given:
DC = Duty Cycle = V_{OUT}/V_{IN}
f_{SW} = Switching Frequency
This calculation also accommodates the max ripple/DC requirements for the slope compensation circuit.

The volt-seconds product can be calculated as follows:

$$V*S = V_I \times dt$$

Given:
V_I = the inductor voltage ($V_{IN} - V_O$)
dt = $V_O/(V_{IN} \times f_{SW})$
Allow sufficient derating to prevent saturation and/or overstress when selecting the inductor.

SELECTING THE MOSFETS

A compromise between conduction loss and transition loss is recommended for the top MOSFET (forward switch). The bottom MOSFET's (synchronous rectifier) power dissipation is dominated by the conduction loss. For highest efficiency, keep the total power dissipation in each switch as low as possible. Conduction loss is a function of $R_{DS(ON)}$, and transition loss is a function of C_{RSS}. The transition losses become more significant as input voltages and switching frequency rise.

Gate charge losses are dissipated in the MSK5055RH and gate resistors if used. Gate charge is related to $R_{DS(ON)}$ and transition time. The power dissipated in the MSK5055RH and gate resistors due to gate charge by each MOSFET can be approximated by the following equation:

$$P_{D(GATE\ DRIVE)} = Q_G \times V_G \times F_{SW}$$

Given: Q_G = Gate Charge
V_G = Gate Drive Voltage
F_{SW} = Switching Frequency

Parasitic FET capacitances can couple the negative switch node transients onto the bottom MOSFET gate drive pin of the device, which could exceed the absolute maximum rating for the pin. A Schottky catch diode rated for 1A is recommended connected to ground to protect the pin from these transients.

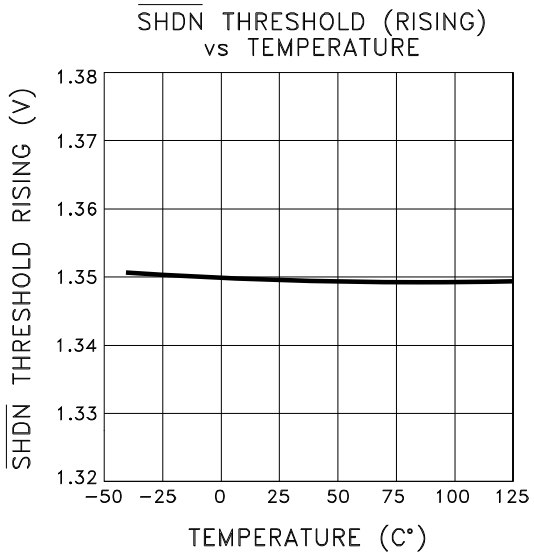
TOTAL DOSE RADIATION TEST PERFORMANCE

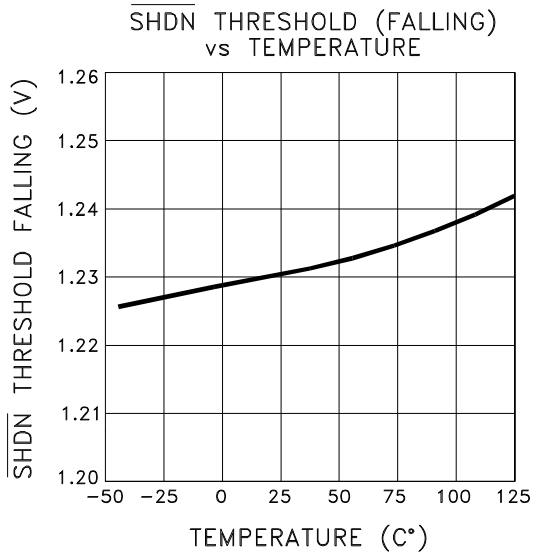
Radiation performance curves have been generated for all testing performed by M.S. Kennedy. These curves show performance trends throughout each test process, and are located in the MSK5055RH radiation test report. The complete test report as available in the RAD HARD PRODUCTS section of the MSK website.

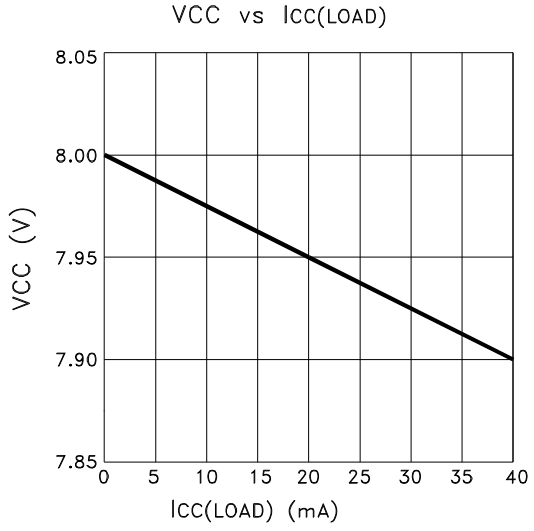
ADDITIONAL APPLICATION INFORMATION

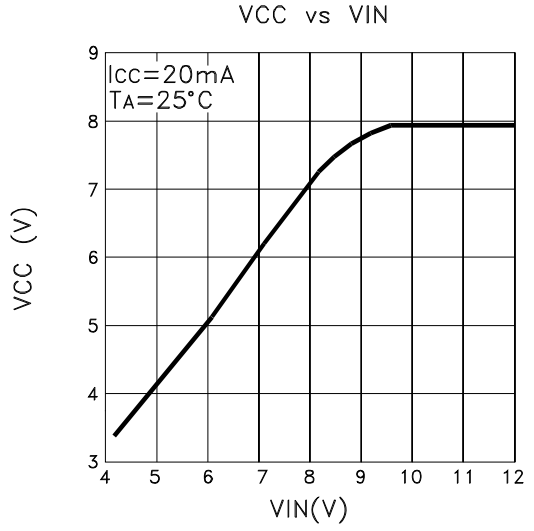
For additional applications information, please reference Linear Technology's® LT3845 data sheet.

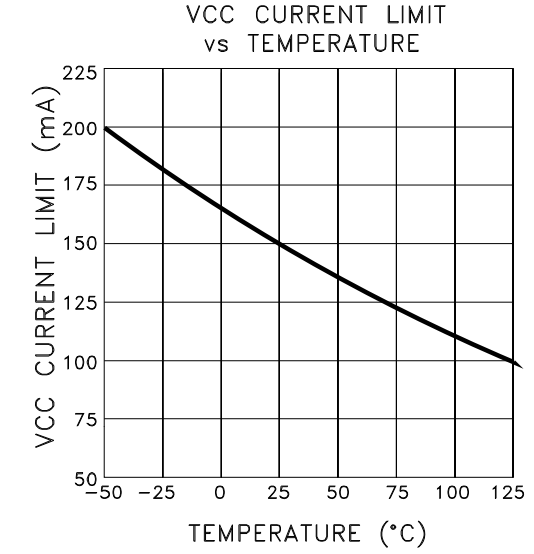
TYPICAL PERFORMANCE CURVES

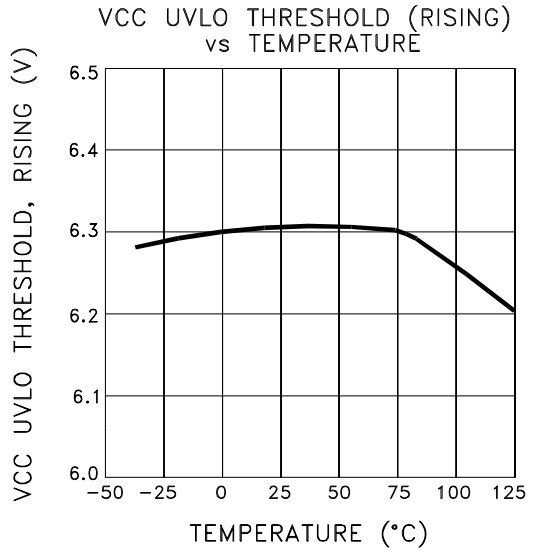




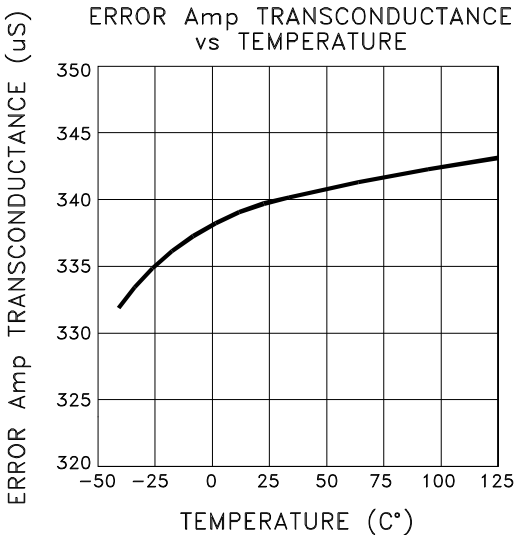


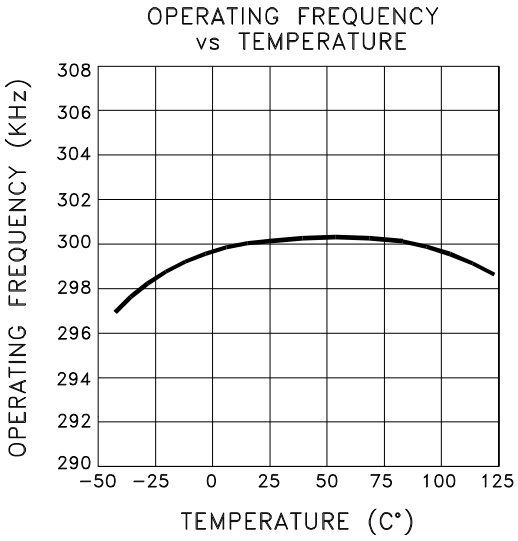


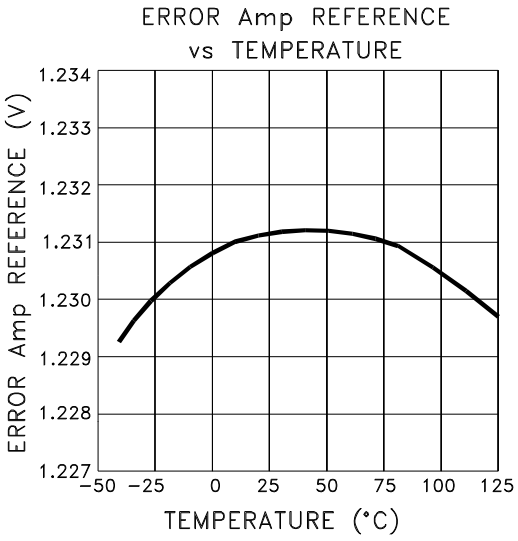


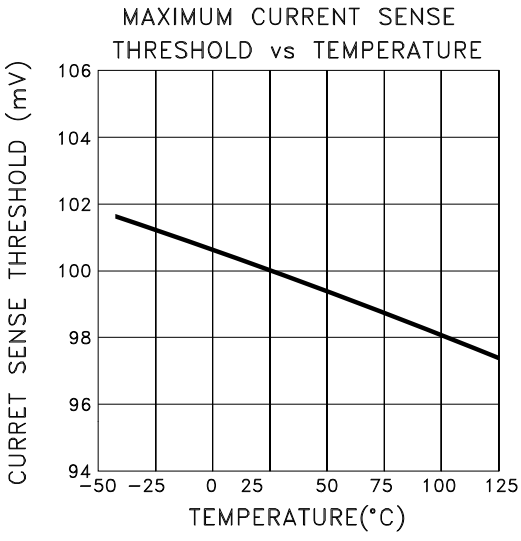


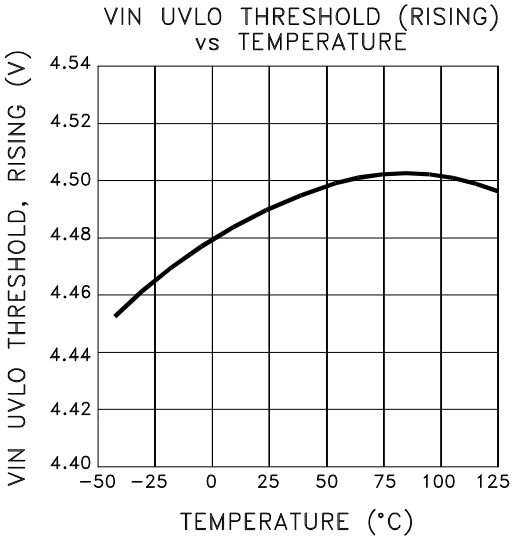
TYPICAL PERFORMANCE CURVES CONT'D

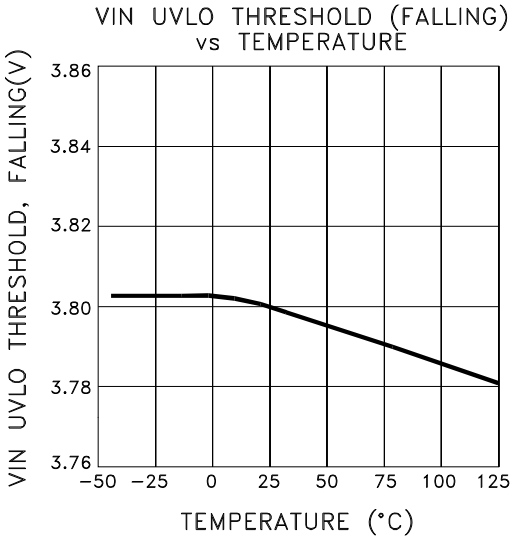




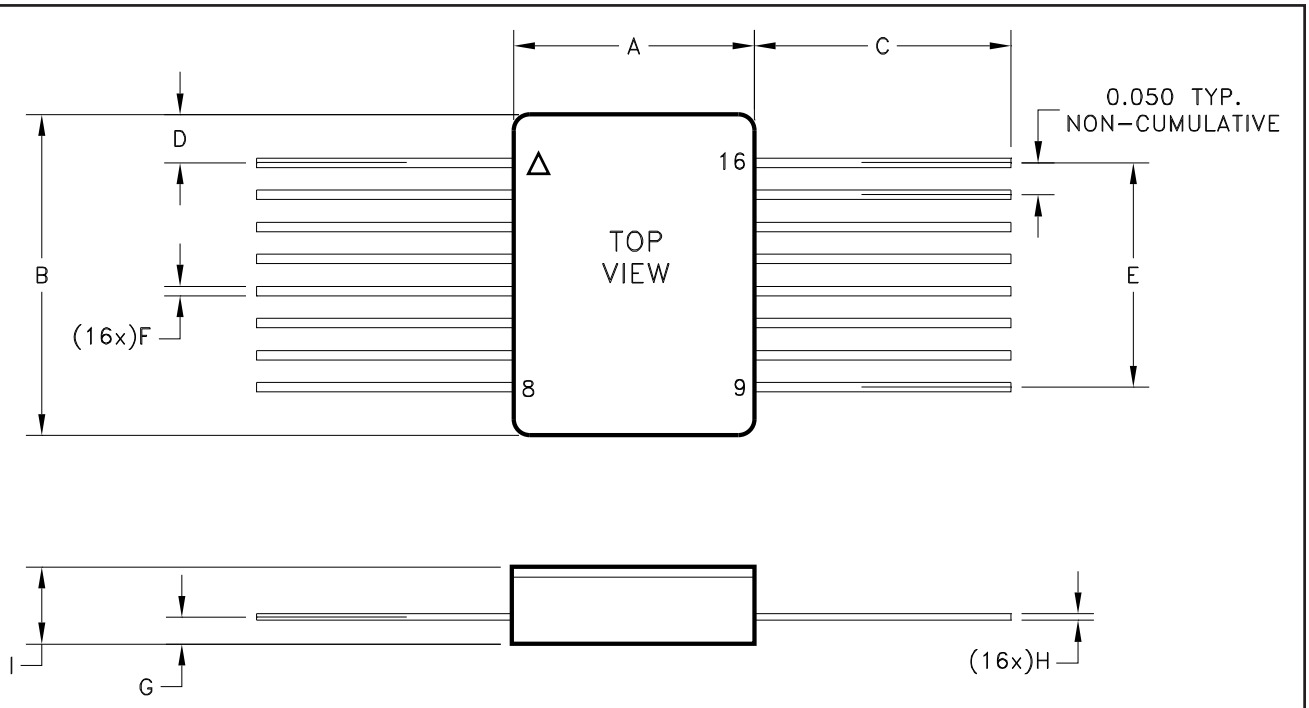








MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	0.365	0.385
B	0.490	0.510
C	0.400	———
D	0.075 REF	
E	0.345	0.355
F	0.012	0.018
G	0.032	0.052
H	0.008	0.012
I	———	0.115

ESD TRIANGLE INDICATES PIN 1
WEIGHT = 1.5 GRAMS TYPICAL

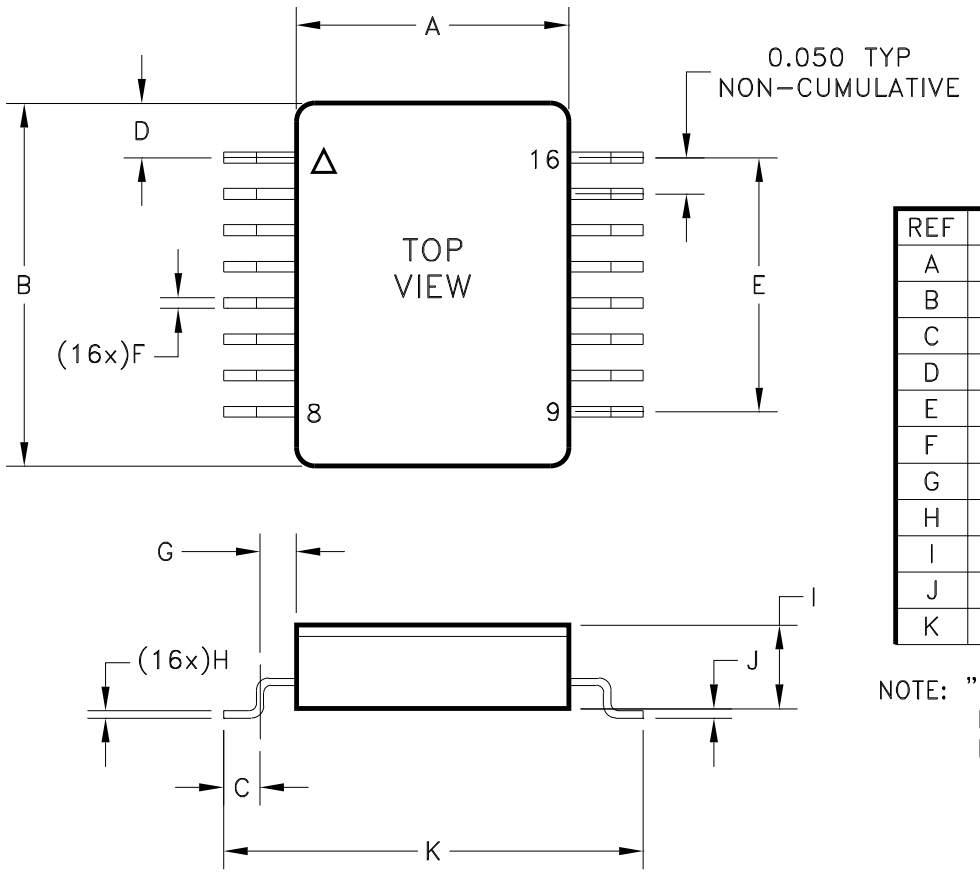
ORDERING INFORMATION

MSK5055- 1 K RH

LEAD CONFIGURATIONS
BLANK = STRAIGHT
RADIATION HARDENED
SCREENING
BLANK = INDUSTRIAL; H = MIL-PRF-38534 CLASS H;
K = MIL-PRF-38534 CLASS K
VERSION
-1 = DCM; -2 = CCM
GENERAL PART NUMBER

The above example is a DCM, Class K regulator controller with straight leads.

MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	0.365	0.385
B	0.490	0.510
C	0.045	0.055
D	0.075 REF	
E	0.345	0.355
F	0.012	0.018
G	0.050 REF	
H	0.008	0.012
I	———	0.115
J	0.008	0.018
K	0.550	0.600

NOTE: "J" IS MEASURED FROM BOTTOM OF PIN TO BOTTOM OF CASE.

ESD TRIANGLE INDICATES PIN 1
WEIGHT = 1.5 GRAMS TYPICAL

ORDERING INFORMATION

MSK5055- 1 K RH G

LEAD CONFIGURATIONS
G = GULL WING
RADIATION HARDENED
SCREENING
BLANK = INDUSTRIAL; H = MIL-PRF-38534 CLASS H;
K = MIL-PRF-38534 CLASS K
VERSION
-1 = DCM; -2 = CCM
GENERAL PART NUMBER

The above example is a DCM, Class K regulator controller with gull wing formed leads.

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